Large-Signal MESFET Characterization Using Harmonic Balance

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Abstract

A method is described that combines large-signal load tuning (i.e., *load-pull*) measurements with harmonic balance and optimization techniques to characterize GaAs MESFET devices. An important advantage of the method is that device model parameters are obtained at the frequencies at which the device will operate in circuits. Consequently, ambiguities regarding any frequency dependencies of the parameters are eliminated, thereby improving the accuracy of the device model and simulation. The method is best suited as a supplement to previously reported DC and small signal parameter extraction methods.

Introduction

During the past two years, significant advances have taken place in CAD for nonlinear microwave circuits. The harmonic balance technique has been shown to be especially promising for predicting the nonlinear behavior of high frequency circuits operating in the steady state. However, despite the power of this technique, its usefulness will be limited by the nonlinear device models employed in the computations.

Unfortunately, many large-signal MESFET models now used in nonlinear analyses are limited not in their structure and analytical framework, but in the methods used to characterize the model parameters. For example, DC parametric I-V data are often used to characterize a device that will operate at microwave frequencies. An inherent assumption is that the parameters describing the device's I-V behavior at DC remain the same at microwave frequencies. However, experiment has shown that many DC parameters, such as the MESFET drain to source conductance, does in fact exhibit significant frequency dependence. The characterization of the device would therefore appear preferable at or near the device's intended frequency of operation. To this end we describe a procedure that provides for the large-signal characterization of devices at microwave frequencies. The method combines innovations in both automated load-pull measurements and harmonic balance techniques.

Method

A) Small Signal Characterization

The procedure begins by fitting a small-signal model to S-parameter data from the device under test (DUT). Careful attention is given to deembedding fixture parasitics from the S-parameter data. Figure 1 depicts a typical lumped-parameter model, which is representative of a broad class of MESFET's. The parameters R_G, R_D, and R_S are port resistances related to the device's structure, process, and packaging. These resistance parameters are obtained, when possible, by DC measurements described by Fukui[1]. The parameters C_A, C_B, C_C, C_D, L_G, L_D, L_S represent parasitic parameters associated with the device's structure and packaging, and are presumably unchanged (as are the above resistances) under large-signal conditions.

We obtain the above capacitive and inductive parasitics by fitting the zero drain voltage S-parameters data to a simplified version of the model in Figure 1 [2]. Once all parasitics and port resistances are acquired, the model of Figure 1 is fitted to S-parameter data from the DUT under bias conditions representative of the real circuit conditions. All fitting is performed using a linear circuit simulator (in our case *MIDAS*[3]).

B) DC Parameter Extraction

In order to provide an initial guess of the model parameters associated with the nonlinear performance of the DUT, DC I-V data from the device is obtained using a transistor curve tracer. This data is then fitted to a large-signal MESFET model. For purposes of illustration, we have employed the Curtice-Ettenberg MESFET model [2]. The model was fitted to I-V data from a Fujitsu FLC30 power MESFET. Figure 2 shows that the model well approximates the DC characteristics of the device. The fitting was performed using a modified version of the Levenberg-Marquardt algorithm [5], and the proprietary in-house program *MESFIT*.

C) Large-Signal Measurements

Large-signal measurements are performed using the conventional "load-pull" procedure, where the output power from a device is monitored as a termination impedance is varied. To expedite the measurements, we use an automated tuning system; the system is commercially available and has been described elsewhere[6]. A manual tuner, however, is equally applicable for the procedure. During the measurements, the device is mounted in a conventional microstrip fixture and wired in the common source configuration (any configuration, however, may apply). Note that wafer probing techniques for direct load-pull measurements on wafer-based devices are equally applicable. In either case, all fixture or probe characteristics are calibrated out using conventional S-parameter correction techniques.

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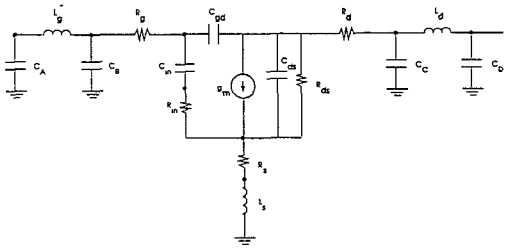

Figure 1. *Small-signal equivalent circuit for MESFET. This model is consistent with the large-signal model used in the analysis*[4].

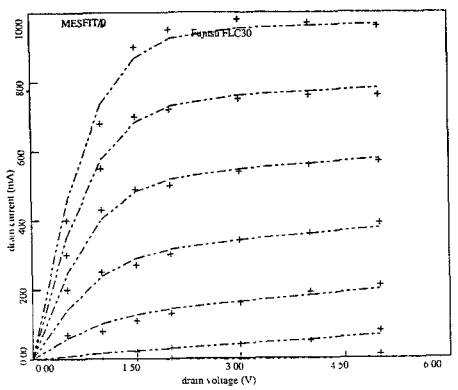

Figure 2. *Fit of Curtice-Ettenberg model to Fujitsu FLC30 power MESFET. Nonlinearity parameters acquired from this fit serve as an initial guess to the large-signal harmonic balance fit;* A_0*=1112.0,* A_1*=242.8,* A_2*=-127.1,* A_3*=-30.15,* β*=0.02,* γ*=1.03.*

After supplying the appropriate biasing, an input signal at the desired frequency of operation is applied to the device's gate. A double-slug tuner is connected to the drain and tuned to produce output load impedance contours on a Smith chart that correspond to constant device power output. The searches are performed at a variety of input powers and DC bias conditions (particularly those conditions to be nominally experienced by the device in the final circuit). All load impedance data, with accompanying power output and bias conditions are collected and sent to the routines described below. Figure 3 shows a typical set of data obtained from the FLC30 device. In the measurements described here, the input impedance as seen by the device was held nominally at 50 ohms; however, an additional tuner may be used to tune the input for maximum power delivered to the device.

Large-Signal Model Fitting

In order to fit any large-signal MESFET (or other device) model to the loadpull data described above, an accurate simulation of the measurement is required. The simulation must account for a variety of factors, including: 1) device parasitics, which are obtained from the small-signal data as described above; 2) device nonlinearities, as obtained from the large-signal model in use; and 3) the impedance of the double-slug tuner at the fundamental and harmonic frequencies (discussed in more detail below). With these three factors considered, loadpull measurement simulations were performed using the harmonic balance simulator *NANA* (for Nonlinear ANAlysis)[7].

Figure 4 shows the results of such a simulation, corresponding to the measurement conditions that generated the data in Figure 3. Considering that DC data was used to describe the nonlinearities of the device in this simulation, the calculated and measured data are quite close and show similar trends. We now aim to adjust parameters of the large-signal model so that the simulations approximate the measurements even more closely. Adjustable large-signal parameters in the Curtice-Ettenberg model include those found in the following equations which relate gate voltage V_1 and drain-source current I_{ds}:

$$I_{ds} = (A_o + A_1 V_1^2 + A_1^3)\tanh(\gamma V_{out}(t)) \quad (1)$$

and

$$V_1(t) = V_{in}(t-\tau)\times[1+\beta(V_{out}^o - V_{out}(t))] \quad (2)$$

where the terms A_i, β, and γ are empirical parameters obtained by DC I-V trace data; these parameters are adjusted during the large-signal fit. Note that the above relations are expressed in the time domain. During the harmonic balance analysis, these relations are also evaluated in the time domain, along with nonlinear gate-source, gate-drain, and drain-source capacitance effects, and drain-gate breakdown effects.

Other parameters that are also adjusted under large signal conditions are the drain-gate feedback capacitance, gate-source and drain-source capacitances, and the drain-source resistance. Starting values for these components are obtained from the fitting of the circuit in Figure 1 to the small-signal data. Note that avalanche breakdown and input saturation effects were assumed negligible during the measurements and simulations.

During the simulations, the load impedance (i.e., tuner impedance model) is set to a series of arbitrarily selected impedance points from among the measured results. Once the simulation for each of the measurement load points is completed, the resulting simulated power output $P_{s,i}$ is compared to the measured power output $P_{m,i}$ at the i^{th} load impedance point. The nonlinear model parameters are then adjusted in such a manner as to minimize the relation:

$$\sum_{i=1}^{n}(P_{m,i}^2 - P_{s,i}^2) \quad (3)$$

We presently use a variation of the Levenberg-Marquardt algorithm to perform the fit[5]. Figure 5 shows the resulting set of simulated contours after a fitting run. These curves were obtained by fitting the selected parameters of the Curtice-Ettenberg model to 17 arbitrarily selected load impedance points from the data in Figure 3. The peak power point and contours were generated using impedance search algorithms described elsewhere[8]. Figure 6 compares P_{in}-P_{out} results for harmonic balance simulations based on the fitted parameters and measurements. The two sets of data are sufficiently close for most design purposes, and perhaps be made to agree even better through the use of newer large-signal models.

Double-Slug Tuner Model

In order to accurately compare the harmonic balance simulations with measurements where the device output is loaded by a tuner, harmonic impedances of the tuner must be accounted for. Alternatively, harmonics that cannot be carefully accounted for during simulation should be filtered during the measurements (this latter procedure, however, still requires an accurate knowledge of the filter's characteristics). For experimental simplicity, we have chosen the first method by modeling the double-slug tuner used in our measurements.

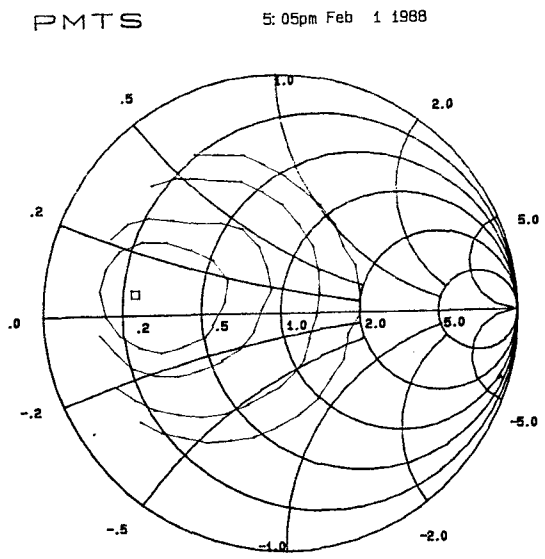

Figure 3. *Loadpull contours and peak power output for FLC-30 device, as measured using an automated tuning system. The contours were generated by varying the impedance of a double-slug tuner. Measured peak output power was 24.2 dBm; contours were for power levels .5, 1, 2, and 3 dB below peak.*

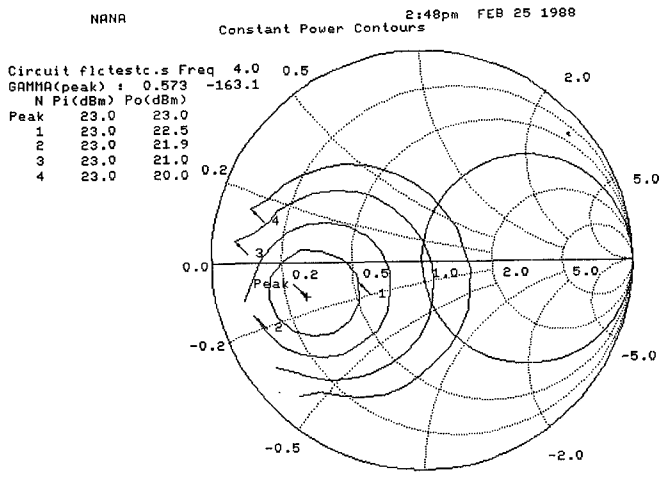

Figure 4. *Simulation of FLC30 using the NANA* harmonic balance program, with parameters obtained from the small-signal circuit fit (Fig. 1) and DC I-V data (Fig. 2).

A cross-section of the tuner is shown in Figure 7. The tuner essentially consists of a slab line with two series dielectric slugs surrounding the center conductor of the line. By varying the relative separation between the slugs, and their distance from the tuner's reference plane, a wide range of impedances can be generated by the tuner. This range may be increased by loading the slugs with a metallic core, as shown in Figure 7. Algorithms to specify slug position along the line for a given fundamental frequency impedance are explained in detail elsewhere[8].

The tuner is electrically modeled by the cascaded transmission line circuit of Figure 8. Each section of the model represents tuner transmission line sections with and without the slugs. As the slug positions change, the relative lengths of the slug-free sections also change. The effective impedance of the cascade is calculated at the fundamental and harmonic frequencies to model the tuner's impedance. Effective line and slug dielectric losses are accounted for in the calculations.

Summary

A method has been described for determining the electrical parameters of a large-signal model representing MESFET devices. The method correlates load impedance data to the results of harmonic balance simulations to evaluate the model's parameters. Once the parameters are determined, nonlinear circuit simulators (such as those using harmonic balance) can more reliably predict the performance of circuits that use the characterized devices. As improvements in device models develop, the method should provide even better device characterizations. The method is also applicable for the characterization of other power device types, including BJT's.

Acknowledgement

This work was sponsored in part by the U.S. Air Force, Avionics Laboratory, Wright Paterson Air Force Base, Dayton, OH under contract F33615-85-C-1767. The authors also wish to thank M. Cummings and F. McGinty at the David Sarnoff Research Center for providing the devices, circuits, and valuable assistance for this work.

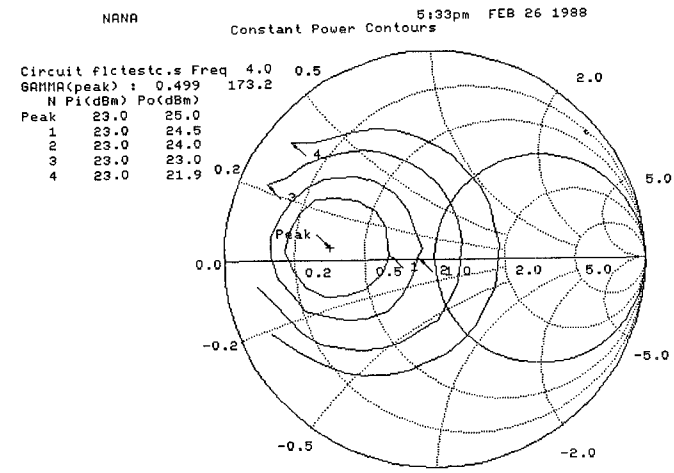

Figure 5. *Simulated FLC30 load contours after large-signal model was fitted to measured contours (Fig. 3); A_0=825.8, A_1=256.4, A_2=-119.0, A_3=-33.99, β=0.005, γ=9.8, total absolute error of fitting 17 equally weighted points was 3.4 dBm.*

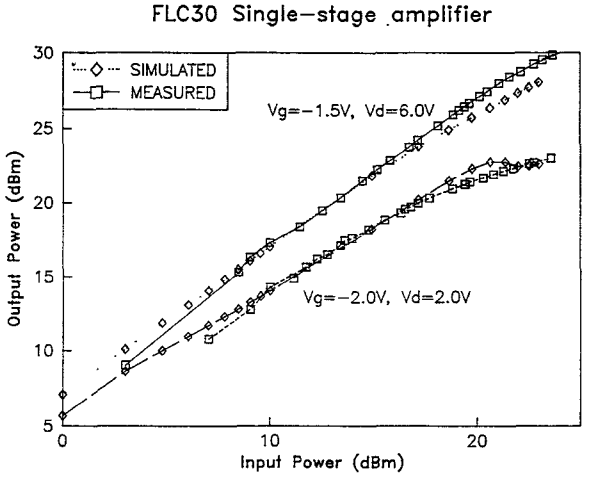

Figure 6. *Comparison of P_{in}-P_{out} measurements and simulations for single-stage power amplifier containing a Fujitsu FLC30. The circuit was designed to match 50 ohm input and output to device at 4.0 GHz. Simulations were based on the parameters extracted from the loadpull contour data.*

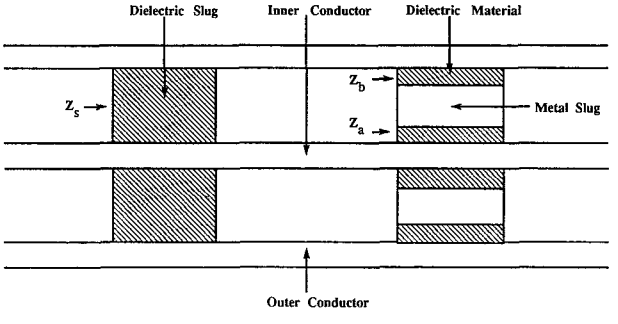

Figure 7. *Cross-section of double-slug tuner used in the measurements and simulations. Dielectric slugs may be made up of pure dielectric, or loaded with a concentric metallic ring to increase the range of tunable impedances.*

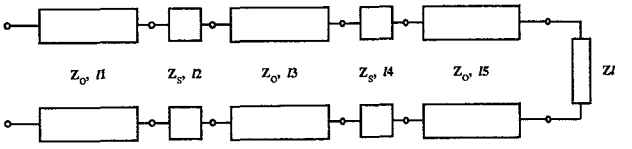

Figure 8. *Transmission line model of double-slug tuner. The tuner's input impedance is modeled by calculating the effective input impedance of the circuit at fundamental and harmonic frequencies.*

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